REMARKS

I. Introduction

In response to the Office Action dated June 3, 2004, claim 11 has been amended. Claims 1-36 remain in the application. Re-examination and re-consideration of the application is requested.

II. Allowable Subject Matter

In paragraph (5), the Office Action indicates that the subject matter of claims 6-8, 11-13, 23, 24, 27, and 28 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicants acknowledge the Office Action's indication of allowable subject matter, but traverse the rejection of the remaining claims.

III. Office Action Objections

In paragraph 1, the Office Action objects to the disclosure because the status of the applications is not recited in the cross-reference. The Applicants have amended the specification to recite the status of the cross-referenced applications.

In paragraph 2, claim 11 is objected to because on lines 3 and 6, the word "multiplier" should be "multiplexer." The Applicants thank the Examiner for noting this error, and have amended claim 11 accordingly.

IV. The Cited References and the Subject Invention

A. The Smith Reference

U.S. Patent No. 3,482,085, issued December 2, 1969 to Smith discloses a binary full adder-subtractor with bypass control. The bypass control has the effect of suppressing the arithmetic operation of the adder-subtractor and causing one of the arguments to the operation to be produced at the output; however, the borrow or carry signal is still produced as if the operation had not been suppressed. The bypass control might be generated, for example, as when a negative difference would be produced by the suppressed operation. The adder-subtractor has particular application in matrix arithmetic units capable of the more complex arithmetic operations of multiply, divide, root taking, power generation, etc., and is preferably constructed of semiconductor logic circuits.

B. The Subject Invention

The present invention, evidenced by an adder for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)* is disclosed. In one embodiment, the adder comprises a bypass input *(bypass)* and a logic circuit, communicatively coupled to the bypass input *(bypass)*, the first input *(A)*, and the second input *(B)*, the logic circuit configured to hold at least one of the first input *(A)* and the second input *(B)* according to the bypass input *(bypass)*. In another embodiment, the present invention is evidenced by an adder for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising a bypass input (*bypass*); and a logic circuit, communicatively coupled to the bypass input (*bypass*), the first input *(A)*, and the second input *(B)*, the logic circuit configured to generate the adder output *(S)* without computing a new adder output according to the bypass input (*bypass*).

C. Differences Between the Subject Invention and the Cited References

Applicants respectfully submit that the two bypassable adder circuits, ours and Smith's, while seemingly similar at a superficial level, are totally different in purpose, in structure, and in operation.

With respect to purpose: The purpose of the Applicants' invention is to create a circuit *that does not dissipate power* in those situations where a new value arrives at one of its input terminals and it is desired to *not* perform the addition operation for the new set of inputs. A second purpose is to provide, as desired in particular applications, the bypass of one of the adder inputs to the output whenever the "no add" situation occurs. Smith, on the other hand, expresses the purpose of providing a conditional bypass capability, but one wherein the output of the carry signal is computed and provided at the adder's carry output terminal just as if the complete adder operation had been performed. This is provided in order that the adder-subtractor have particular application in matrix arithmetic units capable of more complex arithmetic operations. The Smith bypass circuit does not avoid the toggling of logic gates within the adder in those situations wherein a bypass is occurring, as the Applicants' invention does. In fact, by including the additional elements necessary to achieve it's purpose, Smith may well *increase* the power consumption over a standard adder.

Smith does not actually teach "suppressing the arithmetic operations of the adder" as the Office Action suggests on the bottom line of its page 2, but rather, teaches "...*the effect* [emphasis added] of suppressing the arithmetic operation ..." (see the Smith Abstract). This is an important distinction, as Smith does not, in fact, *suppress* the adder's operation but rather, simply modifies its operation so that, logically, it behaves *as if* the summation operation were bypassed. Even in the

bypass mode of operation, Smith's adder still burns power because of the computation it performs to *generate* the "bypass output."

There is a second reason why Smith's adder burns power while in bypass mode ... Smith's adder is generating the *carry* output even in those situations where it is computing a bypass output rather than computing the correct sum.

In contrast, the Applicants' adder *always* avoids burning power when in bypass mode, as that is our primary purpose. The fact that our purpose is the reduction of such power consumption is made evident as it is observed that:

> "A further example of an embodiment of the present invention employs only the holding operation via a bypass control signal without also employing the bypass operation." (Specification, page 50, lines 4-6)

The present invention avoids the consumption of power under bypass control by the use of transmission gates that (conditionally) keep the new input signal value from being presented to the adder circuitry and by, simultaneously, routing signals from within the adder circuitry, back to the adder's input to "hold" the input at its previous value. This causes no adder gates to switch and thereby causes the adder to burn no power.

V. Office Action Prior Art Rejections

In paragraph 4, the Office Action rejected claims 1-5, 9,10,14-22, 25,26, and 29-48 under 35 U.S.C. § 102(b) as unpatentable over Smith. The Applicants respectfully traverse these rejections.

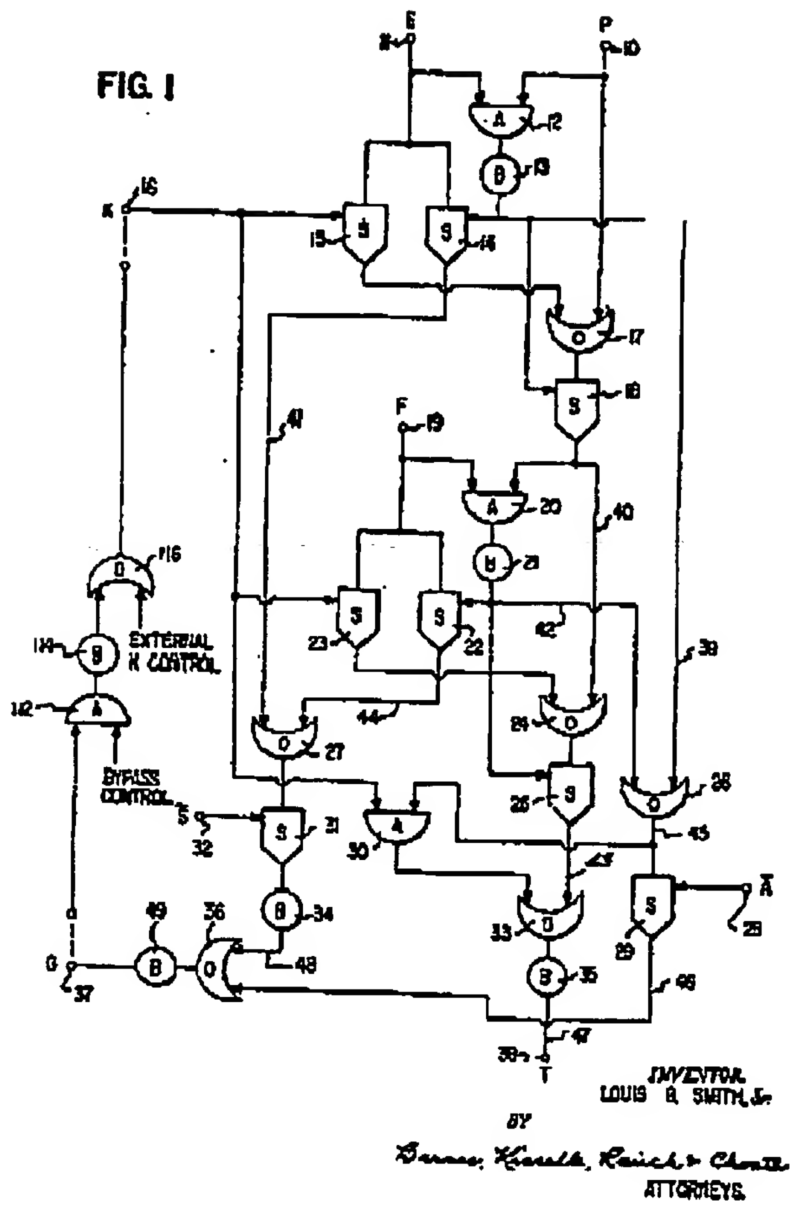
With Respect to Claim 1, 18, 33, 37, and 45: Claim 1 recites:

> An adder for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising:
> a bypass input (*bypass*); and
> a logic circuit, communicatively coupled to the bypass input (*bypass*), the first input *(A)*, and the second input *(B)*, the logic circuit configured to hold at least one of the first input *(A)* and the second input *(B)* according to the bypass input (*bypass*).

According to the Office Action,

> Smith Jr. discloses in figure 1 an adder for adding a first input (E), a second input (P), and a carry input (F) to produce an adder output (T) and a carry out (G). The adder also has a bypass input (K) for controlling the logic of the adder to hold the first input (at 15), the second input (at 18) and the carry input (at 23), and to generate an adder output and carry without computing as claimed (suppressing the arithmetic operations of the adder, see abstract and col. 5, lines 40-71). The element (S, see figure 2d) can be seen as a transmission gate or latch with (a) as a logical input, (b) as clock input, and (c) as an output.

FIG. 1 is reproduced below:



The Applicants respectfully disagree. As described above, the Smith reference does not disclose *a logic circuit that holds at least one of the first input and the second input according to the bypass input*, as recited in claim 1. Instead, Smith teaches a system that modifies the operation of the adder so that it produces an output as if the addition operation were not accomplished. Smith does not "hold" either the first or the second input ... it modifies the logic that uses the first or second input so that it appears to bypass the operation.

The Office Action (on the first line of page 3) states that that:

> "The element (S, see figure 2d) can be seen as a transmission gate or latch with (a) as a logical input, (b) as clock input, and (c) as an output."

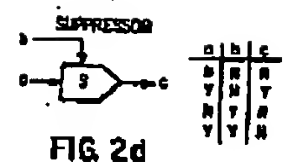
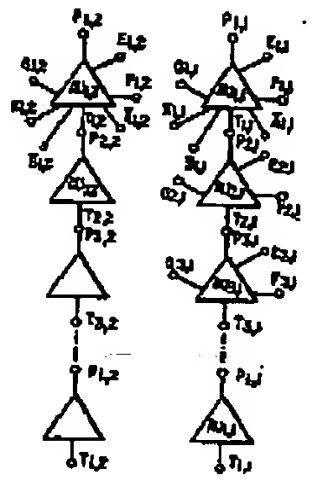


FIG. 2d



The Applicants respectfully disagree. The description of element S (called a SUPPRESSOR) in Smith's figure 2d shows that it is merely a two-input logic function whose output is described by a truth table. A transmission gate, by contrast, provides a high impedance between its input and its output when enabled. This provides the means of disconnecting an input when it is unwanted. No such function occurs in the Smith suppressor; it simply is *not* a transmission gate, nor is it a *latch*. Smith therefore does not disclose a circuit wherein any of its inputs are "held." The Smith suppressor does not disconnect input from output, let alone provide any *input-holding* feature; it merely provides a "logical zero" output signal value whenever enabled.

It is also noted that beyond the crucial difference we've just pointed out regarding the function of Smith's suppressor "S" as distinct from that of a transmission gate—with the consequence that it is unable to *hold* the adder inputs—it is even incorrect to state that Smith's "second input (at 18)" is held by the "bypass input (K)," as is stated in the Office Action (on the fifth and sixth lines of item 4, on page 2), as the enabling signal for suppressor 18 is not associated with bypass input K.

For all the foregoing reasons, the Applicants respectfully traverse the rejection of claim 1.

Claim 18 recites a holding means, and is patentable for the same reason. Claim 18 further recites additional structure not disclosed in the Smith reference.

Likewise, claim 33 recites the step of holding at least one of the first and second inputs according to the bypass. Claim 33 is therefore also patentable over the Smith reference for the same reasons.

Claim 37 recites a second logic circuit element that conditionally holds one of the inputs $A, B, \cdots$ according to the bypass input, as well as other structural features not described in the Smith reference. Claim 37 is therefore patentable on the same basis.

Claim 45 recites the step of conditionally holding one of the inputs $A, B, \cdots$ according to the bypass input. Claim 45 is therefore patentable as well.

With Respect to Claims 14 and 29: Claim 14 recites:

> A device for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising
>
> a bypass input (*bypass*); and
>
> a logic circuit, communicatively coupled to the bypass input (*bypass*), the first input *(A)*, and the second input *(B)*, the logic circuit configured to generate the adder output *(S)* without computing a new adder output according to the bypass input (*bypass*).

According to the Office Action's analysis, inputs A and B correspond to Smith's E and P inputs, respectively. However, Smith's suppressor 18 is not associated with bypass input K, and is not positioned such that it plays any role in suppressing input P. Further, Smith's circuit is not configured to generate the adder output without computing a new adder output. Instead, Smith always computes a new adder output. The logic used to compute the adder output emulates that the computations never took place, but a new adder output is computed nonetheless. Accordingly, claim 14 is patentable over the Smith reference.

Claim 29 recites features analogous to those of claim 14 and is patentable on the same basis.

VI. Dependent Claims

Dependent claims 2-5, 9-10, 15-17, 19-22, 25, 26, 30-32, 34-36, 38-44, and 46-48 incorporate the features of their related independent claims, and are therefore patentable on this basis. In addition, these claims recite novel elements even more remote from the cited references. For example, with respect to claims 5, 10, 22, and 26, the Smith reference does not disclose a transmission gate adder, as described above.

VII. Conclusion

In view of the above, it is submitted that this application is now in good order for allowance and such allowance is respectfully solicited. Should the Examiner believe minor matters still remain that can be resolved in a telephone interview, the Examiner is urged to call Applicants' undersigned attorney.

Respectfully submitted,

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